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EXAMINER	
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2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/936,320	CHU, JACK OON	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *89-98 and 124* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *89-98 & 124* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' amendment faxed on November 2, 2005 has been entered and forwarded to the examiner on November 29, 2005.

Therefore claim 89 as amended by the amendment and claims 90-98 and 124 as previously recited are currently pending in the Application.

Claims 1-88, 99-123 and 125-140 have been cancelled by the amendment.

Election/Restrictions

Applicants' response of November 02, 2005 affirming their election without traverse of claims 89-98 and 124 is noted.

Applicants' timely cancellation on non-elected claims 1-88,99-123 and 125-129 is appreciated.

Information Disclosure Statement

No further IDS after the one filed on Oct. 21, 2004 (which was considered and a copy of the PTO-1449 mailed with the previous O/A) have been filed in this case.

Claim Objections

Claims 94 and 97-98 are objected to because of the following informalities:

Claims 94,97 and 98 recite " third layer is commensurate having a thickness below.." (cls. 94 and 98) ; "thin strain commensurate Si layer" (cl.97) .

It is not understood what Applicants' intend to include/exclude by the above expression .

. Appropriate correction is required.

Claim Rejections - 35 USC Section 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action'.

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 89-98 and 124 are rejected under 35 U.S.C. 102 (b) as being anticipated by Murakami et al. (U.S. Patent No. 5,241,197, herein after Murakami) (also listed by Applicants' in their IDS and cited by Examiner Rao in corresponding PCT).

With respect to claim 89 Murakami describes a layered structure for forming a Ge channel field effect transistors comprising : a single crystalline substrate, (Figure 2A # 1, col.. 3 lines 40, col. Col.2 line 58) a first layer of relaxed Sil-xGex formed epitaxially on said substrate where Ge fraction ranges from about 0.5 to about 0.8, (Figure 28 # 33 , col. 7 lines 16, claim 18) a second layer of Ge formed epitaxially on said first layer (Figure 2 B # 33) whereby said second layer is under compressive strain (figure 10 A) , and having a thickness less than its critical thickness with respect to said first layer, (Embodiment 6 , col. 7 lines 20-25, graphs) a third layer of undoped Sil.xGex formed epitaxially on said second layer, (figure 5 # 55) and a fourth layer of gate dielectric formed on said third layer. (figure 9 B # 86).

With respect to claim 90 Murakami describes the layered structure of claim 89 further including first and second over-shoot layers a Sil m Gem and Sil.nGen, Within a

drain relief structure of said first layer of relaxed Sil.xGex for the case when x is greater than 0.5. (col. 7 lines 16, claim 18 range 0 to 1)

With respect to claims 91 and 92 Murakami describes the layered structure of claim 89 wherein said first over-shoot layer, Sil-mGem, within said strain relief structure of said first layer has a Ge fraction m, where m is the range from 0.05 to less than 0.5. (col. 7 lines 16, claim 18 range 0 to 1)

With respect to claim 93 Murakami describes the layer structure of claim 89 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said second layer having a higher comperisive strain to provide a deeper quantum well or a higher barrier for better hole containment with no alloy scattering ms compared to a single SiGe layer channel device alone. (Embodiment 6 , col. 7 lines 20-25, graphs)

With respect to claim 94 to the extent understood, Murakami describes the layered structure of claim 89 wherein the Ge content of said third layer of Sil-xGm is in the range from 0.5 to 0.8 with a preferred content of 0.30 (col. 7 lines 16, claim 18 range 0 to 1) and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer with a thickness equal to or less than 1 nm. (col.5 lines 29 to 36 and col. 7 line 50 to col. 8 line 36).

With respect to claim 95 Murakami describes the layered structure of claim 89 wherein the Ge content x may be graded with a higher Ge content near said second layer and grading down in Ge content towards the upper surface of said third layer to a value of about 0.30. (Murakami col. 7 lines 50 to col. 8 lines 33).

With respect to claim 96 Murakami describes the layered structure of claim 89 wherein the gate dielectric of said fourth layer is a dielectric material selected from the group consisting of silicon dioxide, silicon oxynitride, silicon nitride, tantalum oxide, barium strontium titanate, aluminum oxide and combinations thereof. (Murakami figs. #86, col.6 line 57-silicon dioxide).

With respect to claims 97 and 98 to the extent understood, Murakami describes the layered structure of claim 89 wherein said third layer of Silicon may be substituted with a thin strained commensurate Si layer suitable for high temperature oxidation in formation of a quality silicon dioxide layer in said fourth layer of gate dielectric. (rejected for reasons stated under claims 94 and 96 above).

With respect to claim 124 Murakami describes the layered structure of claim 89 further including, electrical isolation regions created by the selective removal of at least said fourth layer through said second layer, a gate electrode formed on said gate dielectric of said fourth layer, a source electrode formed and located on one side of said gate electrode, and a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed. (structure of FET see Murakami e.g. figures 9 A , B , etc.).

The claim limitations "electrical isolation regions created bv the selective removal of at least said foudh layer through said second layer, a gate electrode formed on said gate dielectric of said fourth layer, a source electrode formed and located on one side of said gate electrode, and a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed. " in claim 124 are

taken to be product-by -process limitations and non limiting. A product -by -process' claim is directed to the product per se, no matter how actually made . See In re Fessman, 180USPQ 324,326 (CCPA 1974)*, In re Marosi et al., 218 U5PQ289,292 (fed. Cir. 1983)., and padicularly In re Thrope, 227 USPQ 964, 966 (fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product gleamed from the process steps, which must be determined in a " product by process" claim and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in " product by process" claims or not. In conclusion , the process limitations does not change or make the resulting product patentably distinguished over the applied Murakami reference.

Response to Arguments

Applicant's arguments filed 11/29/2005 have been fully considered but they are not persuasive for the following reasons :

Applicants' contention that the Office Action does not establish the anticipation rejection because it allegedly picks, chooses and combines various portions of the disclosure is not persuasive because it is noted that while the Murakami reference describes about 12 embodiments as noted by the Applicants, the embodiments used in the rejection figures 2A to 4 all refer to the first embodiment. (a MODFET and a bipolar transistor) figure 5 (cited in the rejection refers to a second embodiment) describes a similar MODFET to that described in figs. 2 –4 with the only difference that a special type of gate a Schottky gate electrode is used and is an example of doped channel MODFET, however Murakami itself states that "an MOS structure (described in figs. 2

to 4) may be used in place of the Schottky gate structure. " (Murakami col.5 lines 28 to 42, reproduced below).

Although a Schottky gate electrode is used in the MODFET of FIG. 5, an MOS structure may be used in place of the Schottky gate electrode. Further, a channel region including the layers 53, 2, 55 and 52 may be replaced by a superlattice structure where the intrinsic germanium layer and the intrinsic i-$Si_{0.5}Ge_{0.5}$ layer are alternately and repeatedly piled, to increase transconductance g_m.

Although a silicon substrate is used in the present embodiment, a germanium substrate can be used in place of the silicon substrate. Further, various layers of the present embodiment may be formed by the chemical vapor deposition (CVD) method which is excellent for mass production.

Therefore Murakami contrary to Applicants' allegation itself provides for interchangeable uses of embodiments described in figures 2-4 and 5 .

Further Murakami's embodiment described in figure 9 A-B and 10 A to D- (sixth embodiment) and other figures are also interchangeable with the embodiments of other figures like 2,5 etc. because these figures (9 to 10 D) show the doped channel MODFET of figure 5embodiment wherein the doped MODFET of figure 5 is further specified to be a p- channel MODFET.

It is well known in the art that there are only two (2) types of channel p or n both of which are interchangeably used. Therefore it is very clear that the sixth embodiment (figs. 9 to 10 D) can be interchangeably used with the second (2nd) embodiment (figs. 5,etc.) which can be interchangeably used with first embodiment (figs. 2-4).

Further proof that all Of Murakami's embodiments relate to a single invention and are the same interchangeable used is seen from No (species) restriction required in the Application that matured in to the Murakami patent.

Additionally, Murakami's objects on the invention describing all 12 (twelve) interchangeable embodiments provides the common objectives for the invention (reproduced below) .

A transistor according to the present invention uses a high-mobility-carrier transport region as a channel or base, and this region is formed of a germanium layer having a strain. The strain of the germanium layer is controlled by a strain control layer (that is, buffer layer) provided beneath the germanium layer. Preferably, the strain control layer is formed of an $Si_{1-x}Ge_x$ layer. The strain control layer may be provided on both sides of the germanium layer. The strain of the germanium can be controlled by changing the value x of the $Si_{1-x}Ge_x$ alloyed crystal.

It is an object of the present invention to provide a high-speed switching device.

It is another object of the present invention to impose a controlled strain on a germanium layer which provides a carrier transport region.

It is a further object of the present invention to provide a high-performance, heterostructure transistor, in which a layer having large lattice mismatch is formed by strained growth while suppressing the generation of misfit dislocations.

These and other objects and many attendant advantages of the present invention will be readily appreciated and becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings.

Reference is also noted to Murakami col. 2 lines 24 to 50, col. 3 lines 35-40, col. 5 lines 29-42, col. 8 lines 40-45, col. 6 lines 63-68, col. 7 lines 1-10, col. 8 lines 42 to 56, col. 9 lines 4-10, col. 10 lines 30-35, etc. all of which interchangeable uses of the different embodiments.

Therefore contrary to Applicants' contention Murakami itself provides that Murakami structures are similar structures having all of their elements in common that can be inter changeably used and thereafter fine tuning with additional elements added in different embodiments to adjust/"tweak" a particular desired characteristic .

Further Murakami itself at least in the sections stated above clearly shows that the base elements are common to all embodiments and from which desired characteristics are further included in each embodiment by having additional elements that are either added or substituted to emphasis the particular characteristic desired

.Thus providing the motivation and /or suggestion of using different layers/ elements (whenever a particular characteristic has to highlighted) from different embodiments and combine them with the base elements that are common to all embodiments (the particular characteristic and particular motivation set out in great detail in Murakami and not repeated here for the sake of brevity) without using impermissible hindsight, as alleged.

Dependent claims 90-98 and 124 were alleged to be allowable at least for depending upon allegedly allowable independent claim 98 , however as seen above claim 98 is no allowable and therefore dependent claims 90-98and 124 are also finally rejected.

Therefore none of applicants' arguments have overcome the priori art of record.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see hop://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao
Patent Examiner
Jan. 23, 2005.

LONG PHAM
PRIMARY EXAMINER